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(54) **TRANSMITTING CONTROL LINE DRIVER, OLED PANEL HAVING SAME, AND DISPLAY DEVICE**

(52) **U.S. Cl.**
CPC **G09G 3/3233** (2013.01); **G11C 8/08** (2013.01)

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(57) **ABSTRACT**

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A transmitting control line driver, an OLED panel having same, and a display device. The transmitting control line driver comprises multiple stages of transmitting control line driver units. A first time sequence signal transmission line (Ck1) is coupled to first input ends (CKE1) in odd stages of transmitting control line driver units and second input ends (CKE2) in even stages of transmitting control line driver units. A second time sequence signal transmission line (CK2) is coupled to second input ends (CKE2) in the odd stages of transmitting control line driver units and first input ends (CKE1) in the even stages of transmitting control line driver units. A signal output end (out) of each stage of transmitting control line driver unit is coupled to a third input end (in) of a subsequent stage of transmitting control line driver unit.

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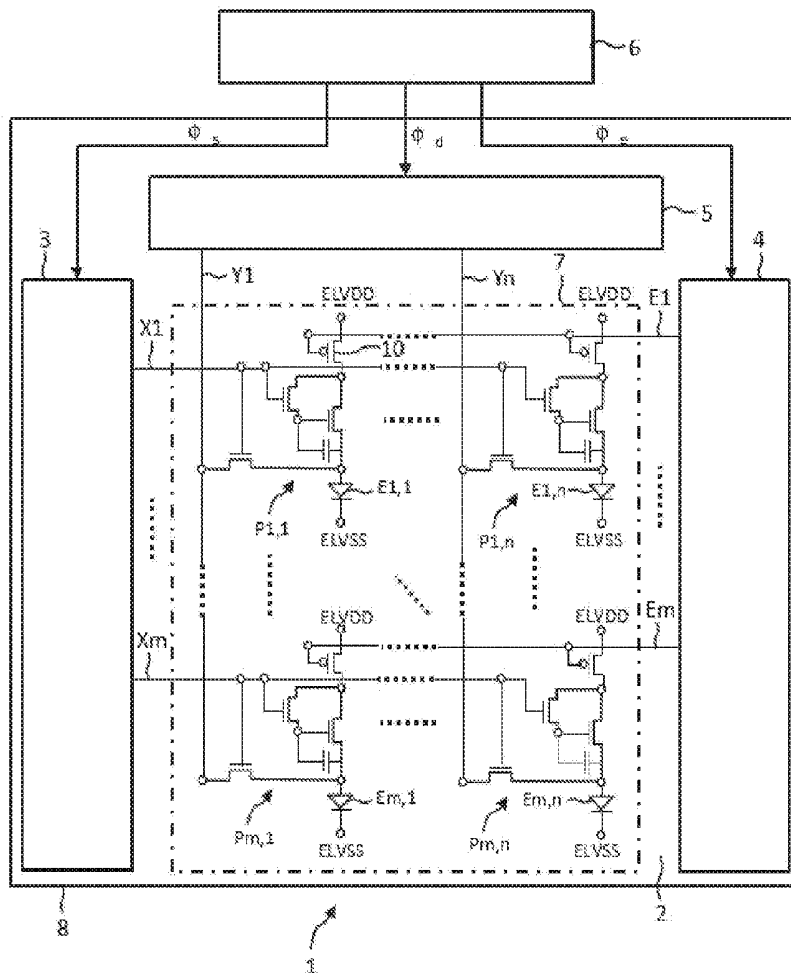
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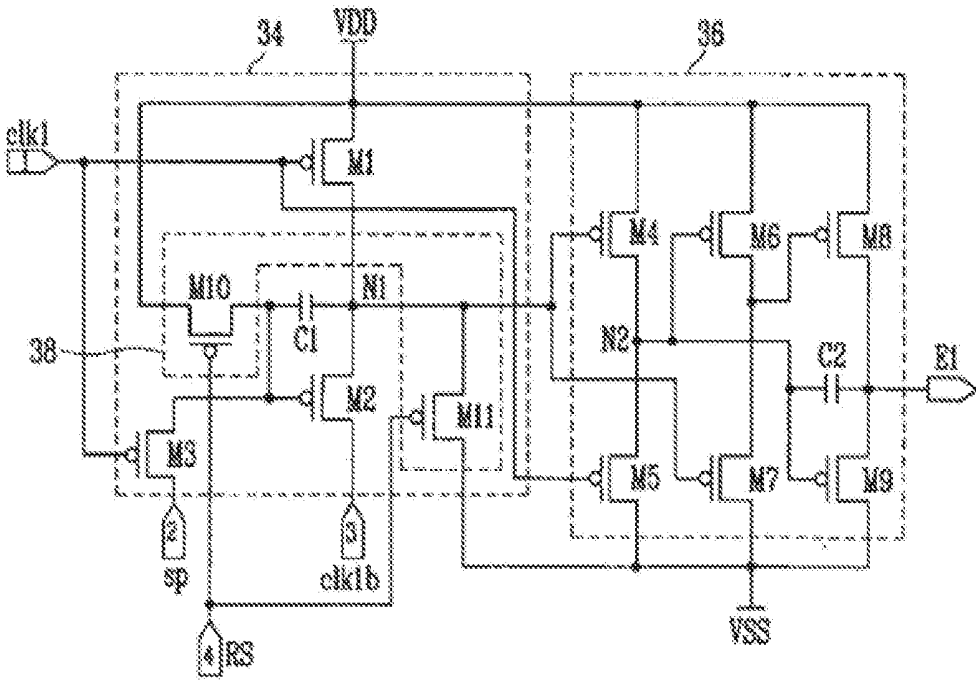


Fig 1

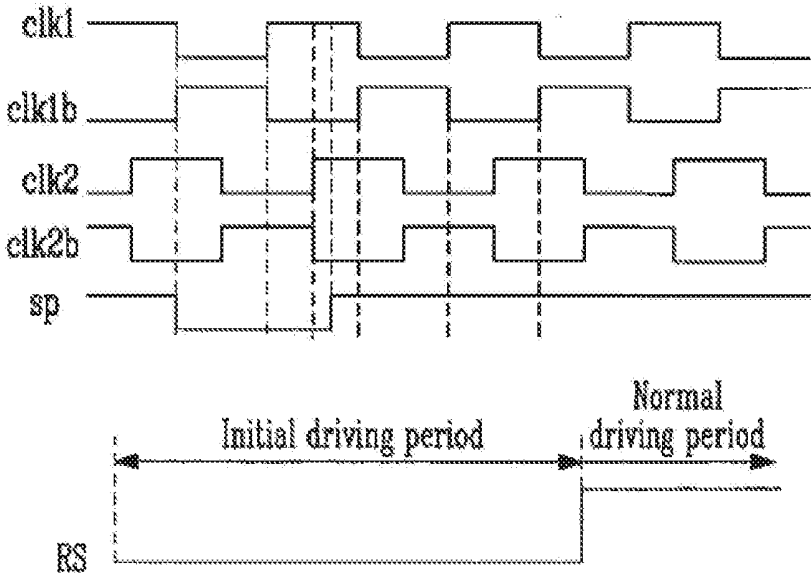


Fig.2

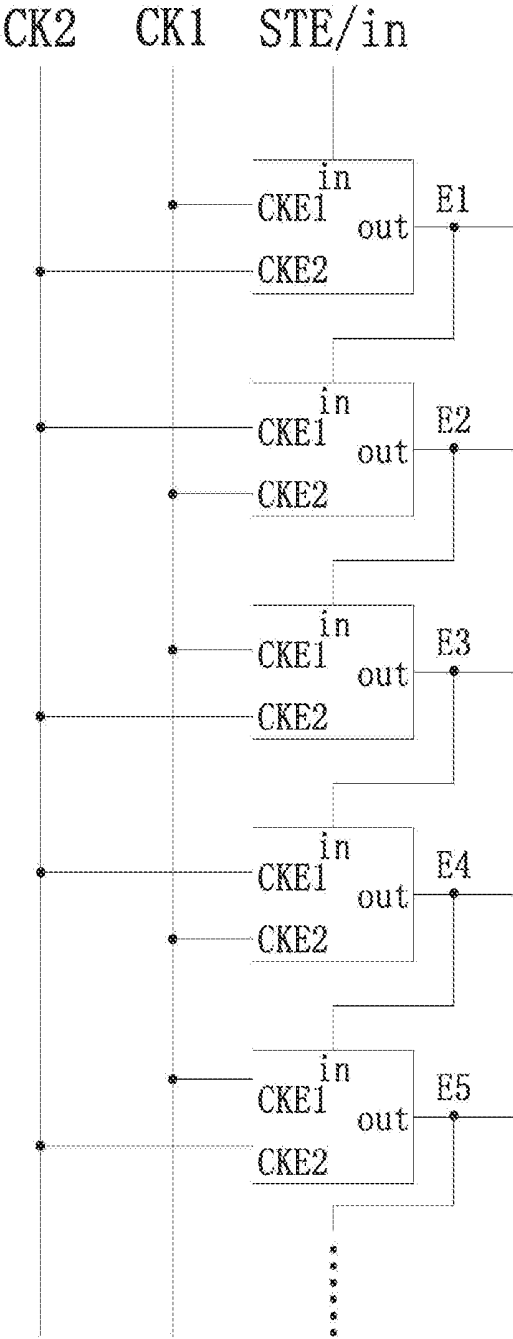


Fig.3

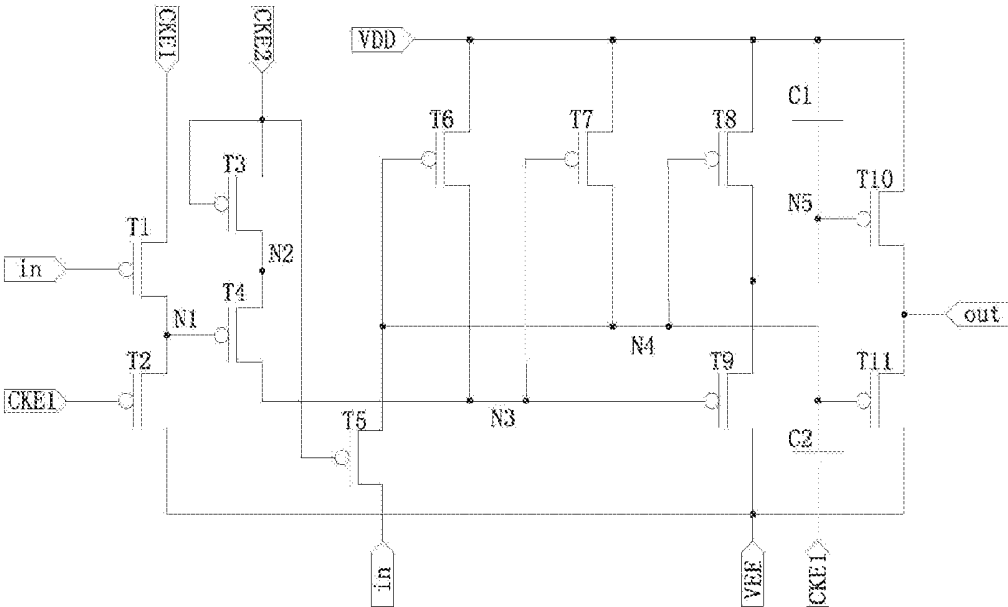


Fig 4

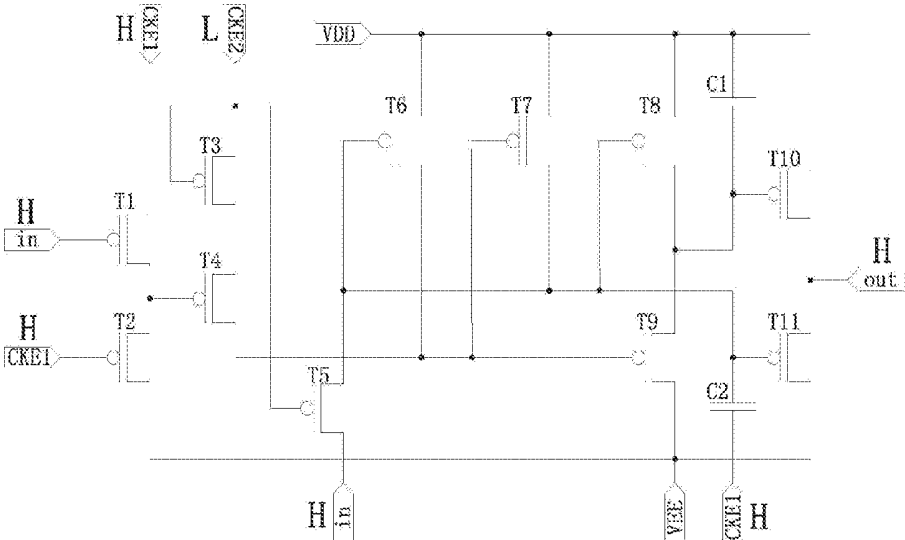


Fig.6

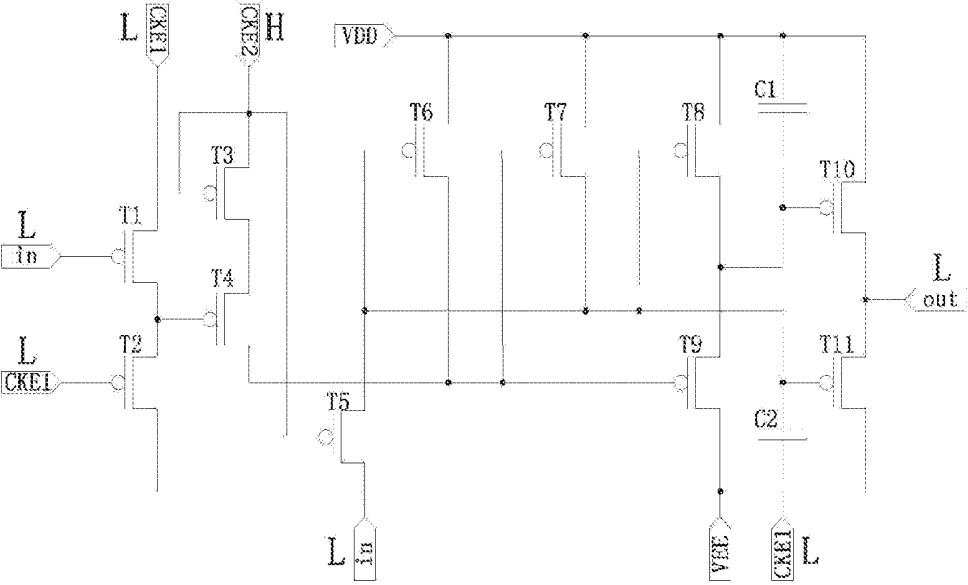


Fig 9

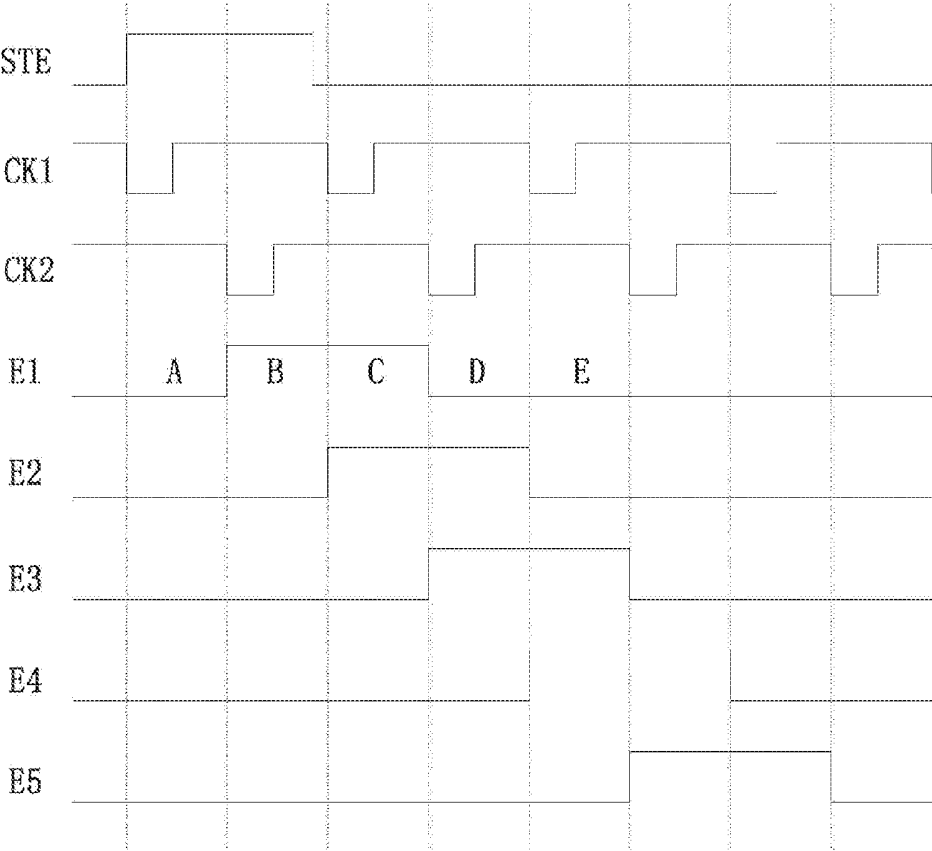


Fig.10

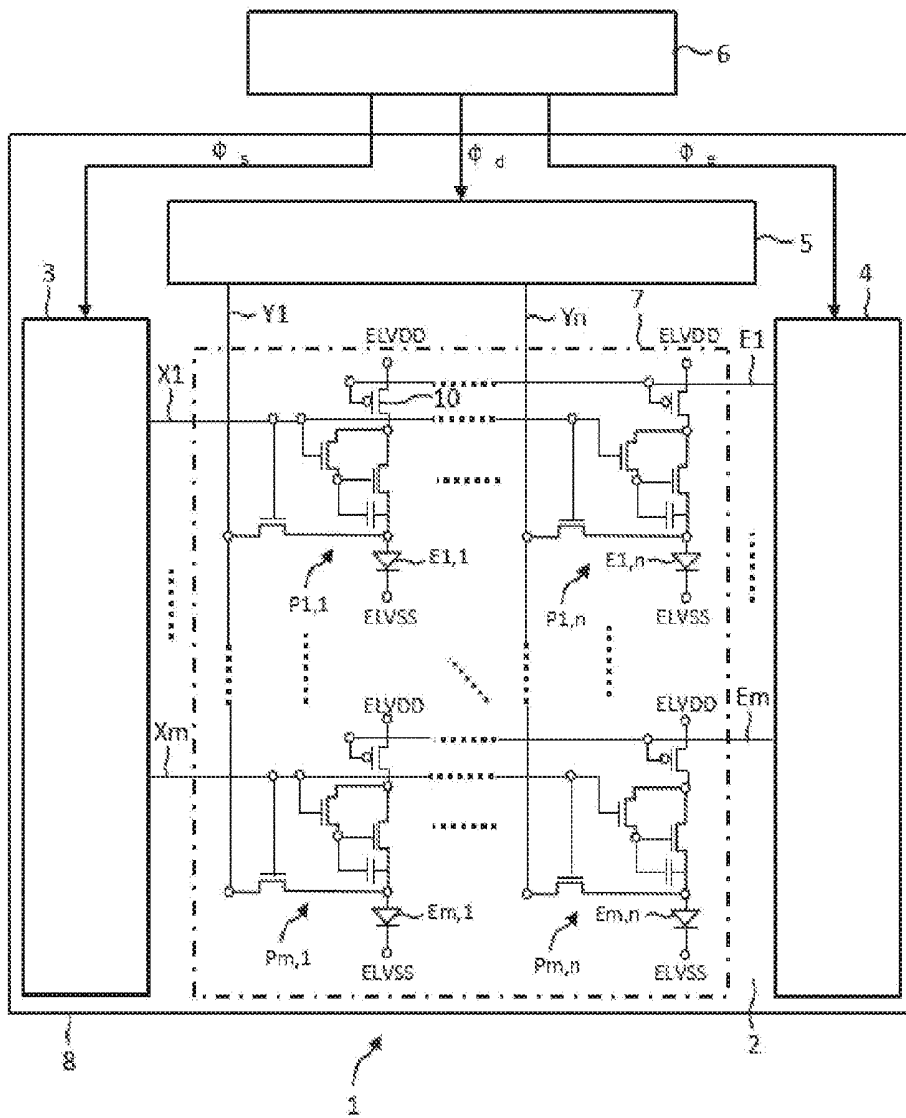


Fig. 11

**TRANSMITTING CONTROL LINE DRIVER,
OLED PANEL HAVING SAME, AND DISPLAY
DEVICE**

TECHNICAL FIELD

[0001] Embodiments of the present disclosure relate to technical field of control circuit for display device, particularly to a transmitting control line driver using two driving signals, an OLED panel comprising the same, and a display device.

BACKGROUND

[0002] Recently, various flat panel displays (FPDs) with smaller weight and size as compared to cathode-ray tube (CRT) display have been developed, including liquid crystal display, field emission display, plasma display panel and organic light-emitting display.

[0003] As a flat panel display, the organic light-emitting display displays images by using organic light-emitting diodes (OLEDs) which emit light by means of recombination of electrons and holes. The organic light-emitting display has a relatively higher response speed and is driven at relatively lower power. A typical organic light-emitting device supplies the OLEDs with current according to data signals by utilizing transistors formed in pixels, so that the OLEDs emit light.

[0004] The typical organic light-emitting display includes: a data driver supplying data lines with data signals, a scan driver supplying scan lines with scan signals sequentially, a transmitting control line driver supplying transmitting control lines with transmitting control signals, and a display unit including a plurality of pixels coupled to the data lines, the scan lines and the transmitting control lines.

[0005] When the scan signal is supplied to the scan line, the pixel included in the display unit is selected to receive the data signal from the data line. The pixel receiving the data line generates light with brightness (e.g., predetermined brightness) based on the data signal and displays a predetermined image. Herein, a transmitting time of the pixel is controlled by the transmitting control signal provided by the transmitting control line. Generally, the transmitting control signal is supplied to be overlapped with the scan signal which is supplied to one or two scan line, so as to configure the pixel supplied with the data line to be at a non-transmitting state.

[0006] The transmitting control line driver includes stages coupled to the transmitting control lines. These stages receive at least four signals, and output high voltage or low voltage to output lines.

[0007] However, the stages included in a typical transmitting control line driver are driven by at least four signals. As illustrated in FIG. 1 and FIG. 2, a circuit of a transmitting control line driver unit of the typical transmitting control line driver includes eleven transistors and two capacitors, and requires at least four signals *clk1*, *clk1b*, *sp* and *rs*; as a result, the circuit has an extremely complex structure, which increases the cost and makes it difficult to ensure the driving reliability.

[0008] The foregoing information disclosed in the BACKGROUND part is merely set forth for facilitating those skilled in the art to understand the background technology of the present disclosure, and hence may contain some infor-

mation which is unknown to those skilled in the art of this country and doesn't constitute the prior art.

SUMMARY

[0009] In view of the defects existed in the prior art, the present disclosure provides a transmitting control line driver and a display device comprising the transmitting control line driver, which overcome the problems in the prior art by modifying the traditional four driving signals to two driving signals without increasing components or elements; in this way, the same function is achieved by using less control signal; the reduce of the control signal can save the area of the circuit diagram, decrease the area of the integrated circuit and also the number of the combined regions, so as to improve the reliability and allow wider operation space for components.

[0010] According to one aspect of the present disclosure, a transmitting control line driver is provided, including multiple stages of transmitting control line driver units, a single-pulse activating signal transmission line, a first time sequence signal transmission line and a second time sequence signal transmission line.

[0011] Each stage of transmitting control line driver unit includes:

[0012] A first transistor coupled between a first input terminal and a first node, the first transistor having a gate electrode coupled to a third input terminal;

[0013] A second transistor coupled between the first node and a first power supply voltage, the second transistor having a gate electrode coupled to the first input terminal;

[0014] A third transistor coupled between a second input terminal and a second node, the third transistor having a gate electrode coupled to the second input terminal;

[0015] A fourth transistor coupled between the second node and a third node, the fourth transistor having a gate electrode coupled to the first node;

[0016] A fifth transistor coupled between a fourth node and an input signal terminal, the fifth transistor having a gate electrode coupled to the second input terminal;

[0017] A sixth transistor coupled between a second power supply voltage and the third node, the six transistor having a gate electrode coupled to the fourth node;

[0018] A seventh transistor coupled between the second power supply voltage and the fourth node, the seventh transistor having a gate electrode coupled to the third node;

[0019] An eighth transistor coupled between the second power supply voltage and a fifth node, the eighth transistor having a gate electrode coupled to the fourth node;

[0020] A ninth transistor coupled between the fifth node and the first power supply voltage, the ninth transistor having a gate electrode coupled to the third node;

[0021] A tenth transistor coupled between the second power supply voltage and a signal output terminal, the tenth transistor having a gate electrode coupled to the fifth node;

[0022] An eleventh transistor coupled between the signal output terminal and the first power supply voltage, the eleventh transistor having a gate electrode coupled to the fourth node;

[0023] A first capacitor coupled between the second power supply voltage and the fifth node; and

[0024] A second capacitor coupled to the fourth node and the first input terminal.

[0025] The signal output terminal of each stage of transmitting control line driver unit is coupled to the third input terminal of a next stage of transmitting control line driver unit.

[0026] The third input terminal of a first stage of transmitting control line driver unit is coupled to the single-pulse activating signal transmission line.

[0027] The first time sequence signal transmission line is coupled to first input terminals of odd number stages of transmitting control line driver units and is coupled to second input terminals of even number stages of transmitting control line driver units.

[0028] The second time sequence signal transmission line is coupled to second input terminals of odd number stages of transmitting control line driver units and is coupled to first input terminals of even number stages of transmitting control line driver units.

[0029] The signal output terminal of each stage of transmitting control line driver unit is coupled to the third input terminal of a next stage of transmitting control line driver unit, respectively.

[0030] Preferably, the first transistor, the second transistor, the third transistor, the fourth transistor, the fifth transistor, the sixth transistor, the seventh transistor, the eighth transistor, the ninth transistor, the tenth transistor and the eleventh transistor are all PMOS transistors.

[0031] Preferably, the first time sequence signal transmission line is configured to transmit a first clock pulse signal; the second time sequence signal transmission line is configured to transmit a second clock pulse signal; and the first clock pulse signal and the second clock pulse signal are not overlapped with each other.

[0032] Preferably, the second clock pulse signal is a half-period delay signal of the first clock pulse signal.

[0033] Preferably, the third input terminal of the first stage of transmitting control line driver unit is configured to receive a single-pulse activating signal.

[0034] Preferably, the signal output terminal of each stage of transmitting control line driver unit is further coupled to a transmitting control line.

[0035] According to another aspect of the present disclosure, an OLED panel is provided, the OLED panel including a signal controller, a data driver, a scan driver, a plurality of OLED pixels and the transmitting control line driver as mentioned above. The transmitting control line driver includes multiple stages of transmitting control line driver units, a single-pulse activating signal transmission line, a first time sequence signal transmission line and a second time sequence signal transmission line.

[0036] Each stage of transmitting control line driver unit includes:

[0037] A first transistor coupled between a first input terminal and a first node, the first transistor having a gate electrode coupled to a third input terminal;

[0038] A second transistor coupled between the first node and a first power supply voltage, the second transistor having a gate electrode coupled to the first input terminal;

[0039] A third transistor coupled between a second input terminal and a second node, the third transistor having a gate electrode coupled to the second input terminal;

[0040] A fourth transistor coupled between the second node and a third node, the fourth transistor having a gate electrode coupled to the first node;

[0041] A fifth transistor coupled between a fourth node and a signal input terminal, the fifth transistor having a gate electrode coupled to the second input terminal;

[0042] A sixth transistor coupled between a second power supply voltage and the third node, the sixth transistor having a gate electrode coupled to the fourth node;

[0043] A seventh transistor coupled between the second power supply voltage and the fourth node, the seventh transistor having a gate electrode coupled to the third node;

[0044] An eighth transistor coupled between the second power supply voltage and a fifth node, the eighth transistor having a gate electrode coupled to the fourth node;

[0045] A ninth transistor coupled between the fifth node and the first power supply voltage, the ninth transistor having a gate electrode coupled to the third node;

[0046] A tenth transistor coupled between the second power supply voltage and a signal output terminal, the tenth transistor having a gate electrode coupled to the fifth node;

[0047] An eleventh transistor coupled between the signal output terminal and the first power supply voltage, the eleventh transistor having a gate electrode coupled to the fourth node;

[0048] A first capacitor coupled between the second power supply voltage and the fifth node; and

[0049] A second capacitor coupled to the fourth node and the first input terminal.

[0050] The signal output terminal of each stage of transmitting control line driver unit is coupled to a third input terminal of a next stage of transmitting control line driver unit, respectively.

[0051] The third input terminal of the first stage of transmitting control line driver unit is coupled to the single-pulse activating signal transmission line.

[0052] The first time sequence signal transmission line is coupled to first input terminals of odd number stages of transmitting control line driver units and is coupled to second input terminals of even number stages of transmitting control line driver units.

[0053] The second time sequence signal transmission line is coupled to second input terminals of odd number stages of transmitting control line driver units and is coupled to first input terminals of even number stages of transmitting control line driver units.

[0054] The signal output terminal of each stage of transmitting control line driver unit is coupled to the third input terminal of a next stage of transmitting control line driver unit.

[0055] Preferably, the first transistor, the second transistor, the third transistor, the fourth transistor, the fifth transistor, the sixth transistor, the seventh transistor, the eighth transistor, the ninth transistor, the tenth transistor, and the eleventh transistor are all PMOS transistors.

[0056] Preferably, the first time sequence signal transmission line is configured to transmit a first clock pulse signal; the second time sequence signal transmission line is configured to transmit a second clock pulse signal; and the first clock pulse signal and the second clock pulse signal are not overlapped with each other.

[0057] Preferably, the second clock pulse signal is a half-period delay signal of the first clock pulse signal.

[0058] Preferably, the third input terminal of the first stage of transmitting control line driver unit is configured to receive a single-pulse activating signal.

[0059] Preferably, the signal output terminal of each stage of transmitting control line driver unit is further coupled to a transmitting control line.

[0060] According to yet another aspect of the present disclosure, a display device is further provided, including a signal controller, a data driver, a scan driver, a plurality of OLED pixels and the transmitting control line driver as mentioned above. The transmitting control line driver includes multiple stages of transmitting control line driver units, a single-pulse activating signal transmission line, a first time sequence signal transmission line and a second time sequence signal transmission line.

[0061] Each stage of transmitting control line driver unit includes:

[0062] A first transistor coupled between a first input terminal and a first node, the first transistor having a gate electrode coupled to a third input terminal;

[0063] A second transistor coupled between the first node and a first power supply voltage, the second transistor having a gate electrode coupled to the first input terminal;

[0064] A third transistor coupled between a second input terminal and a second node, the third transistor having a gate electrode coupled to the second input terminal;

[0065] A fourth transistor coupled between the second node and a third node, the fourth transistor having a gate electrode coupled to the first node;

[0066] A fifth transistor coupled between a fourth node and a signal input terminal, the fifth transistor having a gate electrode coupled to the second input terminal;

[0067] A sixth transistor coupled between a second power supply voltage and the third node, the six transistor having a gate electrode coupled to the fourth node;

[0068] A seventh transistor coupled between the second power supply voltage and the fourth node, the seventh transistor having a gate electrode coupled to the third node;

[0069] An eighth transistor coupled between the second power supply voltage and a fifth node, the eighth transistor having a gate electrode coupled to the fourth node;

[0070] A ninth transistor coupled between the fifth node and the first power supply voltage, the ninth transistor having a gate electrode coupled to the third node;

[0071] A tenth transistor coupled between the second power supply voltage and a signal output terminal, the tenth transistor having a gate electrode coupled to the fifth node;

[0072] An eleventh transistor coupled between the signal output terminal and the first power supply voltage, the eleventh transistor having a gate electrode coupled to the fourth node;

[0073] A first capacitor coupled between the second power supply voltage and the fifth node; and

[0074] A second capacitor coupled to the fourth node and the first input terminal.

[0075] The signal output terminal of each stage of transmitting control line driver unit is coupled to a third input terminal of a next stage of transmitting control line driver unit, respectively.

[0076] The third input terminal of the first stage of transmitting control line driver unit is coupled to the single-pulse activating signal transmission line.

[0077] The first time sequence signal transmission line is coupled to first input terminals of odd number stages of transmitting control line driver units and is coupled to second input terminals of even number stages of transmitting control line driver units.

[0078] The second time sequence signal transmission line is coupled to second input terminals of odd number stages of transmitting control line driver units and is coupled to first input terminals of even number stages of transmitting control line driver units.

[0079] The signal output terminal of each stage of transmitting control line driver unit is coupled to the third input terminal of a next stage of transmitting control line driver unit, respectively.

[0080] Preferably, the first transistor, the second transistor, the third transistor, the fourth transistor, the fifth transistor, the sixth transistor, the seventh transistor, the eighth transistor, the ninth transistor, the tenth transistor, and the eleventh transistor are all PMOS transistors.

[0081] Preferably, the first time sequence signal transmission line is configured to transmit a first clock pulse signal; the second time sequence signal transmission line is configured to transmit a second clock pulse signal; and the first clock pulse signal and the second clock pulse signal are not overlapped with each other.

[0082] Preferably, the second clock pulse signal is a half-period delay signal of the first clock pulse signal.

[0083] Preferably, the third input terminal of the first stage of transmitting control line driver unit is configured to receive a single-pulse activating signal.

[0084] Preferably, the signal output terminal of each stage of transmitting control line driver unit is further coupled to a transmitting control line.

[0085] By virtue of utilizing the above-mentioned technical solutions, as compared with related technology, in the transmitting control line driver of the present disclosure, the traditional four driving signals are reduced to two driving signals without increasing components or elements. In this way, the same function is achieved by using less control signals; with the reduce of the control signals, the area of the circuit diagram is saved, the area of the integrated circuit is decreased and also the number of the combined regions is decreased, the reliability is improved, and wider operating spaces for components is allowed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0086] Other features, objective and advantageous of the present disclosure will be more apparent from the following detailed description with reference to the drawings, in which:

[0087] FIG. 1 illustrates a circuit diagram of a transmitting control line driver unit in a transmitting control line driver provided in the prior art;

[0088] FIG. 2 illustrates an input pulse waveform diagram corresponding to the transmitting control line driver unit in the transmitting control line driver provided in the prior art;

[0089] FIG. 3 illustrates a circuit diagram of a transmitting control line driver of the present disclosure, according to a first embodiment of the present disclosure;

[0090] FIG. 4 illustrates a circuit diagram of a transmitting control line driver unit in the transmitting control line driver of the present disclosure, according to the first embodiment of the present disclosure;

[0091] FIG. 5 illustrates a schematic diagram illustrating a circuit-conducted state of a first stage of transmitting control line driver unit, at a first moment, in the transmitting control line driver of the present disclosure, according to the first embodiment of the present disclosure;

[0092] FIG. 6 illustrates a schematic diagram illustrating a circuit-conducted state of the first stage of transmitting control line driver unit, at a second moment, in the transmitting control line driver of the present disclosure, according to the first embodiment of the present disclosure;

[0093] FIG. 7 illustrates a schematic diagram illustrating a circuit-conducted state of the first stage of transmitting control line driver unit, at a third moment, in the transmitting control line driver of the present disclosure, according to the first embodiment of the present disclosure;

[0094] FIG. 8 illustrates a schematic diagram illustrating a circuit-conducted state of the first stage of transmitting control line driver unit, at a fourth moment, in the transmitting control line driver of the present disclosure, according to the first embodiment of the present disclosure;

[0095] FIG. 9 illustrates a schematic diagram illustrating a circuit-conducted state of the first stage of transmitting control line driver unit, at a fifth moment, in the transmitting control line driver of the present disclosure, according to the first embodiment of the present disclosure;

[0096] FIG. 10 illustrates input pulse waveform diagrams corresponding to respective stages of transmitting control line driver units in the transmitting control line driver of the present disclosure, according to the first embodiment of the present disclosure; and

[0097] FIG. 11 illustrates a circuit block diagram of an OLED panel of the present disclosure, according to the first embodiment of the present disclosure.

DETAILED DESCRIPTION

[0098] Those skilled in the art should be understood that modified examples may be obtained by combining prior art with the foregoing embodiments, and hence will not be described in details herein. These modified examples will not affect the substantive contents of the present disclosure, with details thereof omitted herein.

[0099] Hereinafter the illustrative embodiments will be described more completely. However, these embodiments may be implemented by various ways and should not be construed to be limited to the implementations set forth herein. More accurately, these implementations are provided for purpose of sufficiency and completeness of the contents disclosed by the present disclosure, so that the scope of protection of the present disclosure can be well conveyed to those ordinary skilled in the art.

[0100] For purpose of clarity, dimensions of layers and regions in the drawings may be exaggerated. Similar reference numerals throughout the specification indicate similar elements.

[0101] It should be understood that, although terms such as “first”, “second” and “third” are used to describe various elements, these elements should not be interpreted to be limited to these terms. The above-mentioned terms are merely used for distinguishing an element from another one. Therefore, as discussed hereinafter, a “first element” may be referred to as a “second element” without departing from the technical teaching of the present disclosure. As used herein, the term “and/or” includes any or all combination of one or more correlated items as listed.

[0102] The terms are used herein merely for purpose of describing particular illustrative embodiments but not limiting the inventive concept of the present disclosure. As used in the present disclosure, “a” and “an” in singular forms should also include meanings of plural forms, unless other-

wise defined. It should also be appreciated that, as used in the specification, terms “comprising” and/or “including” specifies the presence of a feature, an integer, a step, an operation, an element and/or a component, without excluding the presence or addition of one or more other feature, integer, step, operation, element, component and/or combination thereof.

[0103] Unless defined oppositely, all terms (including technical terms and scientific terms) as used herein should be interpreted identically with those generally understood by one ordinary skilled in the art. It should also be appreciated that, the terms as defined in, for example, a publically used dictionary, should be interpreted to have meanings consistent with that in the context of related fields, and shall not be interpreted ideally or excessively literally, unless definitely specified so in the present disclosure.

First Embodiment

[0104] As illustrated in FIG. 3 and FIG. 4, the transmitting control line driver of the present disclosure includes multiple stages of transmitting control line driver units (the present embodiment only illustrates a first stage of transmitting control line driver unit E1 through a fifth stage of transmitting control line driver unit E5, without limiting the embodiments thereto); and the transmitting control line driver is controlled by a single-pulse activating signal transmission line, a first time sequence signal transmission line CK1 and a second time sequence signal transmission line CK2. A third input terminal in of the first stage of transmitting control line driver unit is coupled to the single-pulse activating signal transmission line.

[0105] Each stage of transmitting control line driver unit includes first through eleventh p-channel metal oxide semiconductor (PMOS) transistors T1-T11, as well as a first capacitor C1 and a second capacitor C2.

[0106] The first PMOS transistor T1 is coupled between a first input terminal CKE1 and a first node N1, and the first PMOS transistor T1 has a gate electrode coupled to a third input terminal “in”. The second PMOS transistor T2 is coupled between the first node N1 and a first power supply voltage VEE, and the second PMOS transistor T2 has a gate electrode coupled to the first input terminal CKE1. The third PMOS transistor T3 is coupled between a second input terminal CKE2 and a second node N2, and the third PMOS transistor T3 has a gate electrode coupled to the second input terminal CKE2. The fourth PMOS transistor T4 is coupled between the second node N2 and a third node N3, and the fourth PMOS transistor T4 has a gate electrode coupled to the first node N1. The fifth PMOS transistor T5 is coupled between a fourth node N4 and a signal input terminal, and the fifth PMOS transistor T5 has a gate electrode coupled to the second input terminal CKE2. The sixth PMOS transistor T6 is coupled between a second power supply voltage VDD and the third node N3, and the sixth PMOS transistor T6 has a gate electrode coupled to the fourth node N4. The seventh PMOS transistor T7 is coupled between the second power supply voltage VDD and the fourth node N4, and the seventh PMOS transistor T7 has a gate electrode coupled to the third node N3. The eighth PMOS transistor T8 is coupled between the second power supply voltage VDD and a fifth node N5, and the eighth PMOS transistor T8 has a gate electrode coupled to the fourth node N4. The ninth PMOS transistor T9 is coupled between the fifth node N5 and the first power supply voltage VEE, and the ninth PMOS transistor T9 has

a gate electrode coupled to the third node N3. The tenth PMOS transistor T10 is coupled between the second power supply voltage VDD and a signal output terminal “out”, and the tenth PMOS transistor T10 has a gate electrode coupled to the fifth node N5. The eleventh PMOS transistor T11 is coupled between the signal output terminal “out” and the first power supply voltage VEE, and the eleventh PMOS transistor T11 has a gate electrode coupled to the fourth node N4. The first capacitor C1 is coupled between the second power supply voltage VDD and the fifth node N5. The second capacitor C2 is coupled to the fourth node N4 and the first input terminal CKE1. The signal output terminal “out” of each stage of transmitting control line driver unit is coupled to the third input terminal “in” of a next stage of transmitting control line driver unit, respectively. Moreover, the signal output terminal “out” of each stage of transmitting control line driver unit is further coupled to a transmitting control line.

[0107] The first time sequence signal transmission line CK1 is coupled to first input terminals CKE1 of odd number stages of transmitting control line driver units and is coupled to second input terminals CKE2 of even number stages of transmitting control line driver units. The second time sequence signal transmission line CK2 is coupled to second input terminals CKE2 of odd number stages of transmitting control line driver units and is coupled to first input terminals CKE1 of even number stages of transmitting control line driver units. The signal output terminal “out” of each stage of transmitting control line driver unit is coupled to the third input terminal “in” of a next stage of transmitting control line driver unit.

[0108] In the present embodiment, the first time sequence signal transmission line CK1 is configured to transmit a first clock pulse signal, the second time sequence signal transmission line CK2 is configured to transmit a second clock pulse signal, and the first clock pulse signal and the second clock pulse signal are not overlapped with each other, without limiting the embodiments thereto.

[0109] According to the connecting methods of the transmitting control line driver units, the first input terminal CKE1 of the odd number stage of transmitting control line driver unit is configured to receive the first clock pulse signal, and the second input terminal CKE2 of the odd number stage of transmitting control line driver unit is configured to receive the second clock pulse signal; the first input terminal CKE1 of the even number stage of transmitting control line driver unit is configured to receive the second clock pulse signal, and the second input terminal CKE2 of the odd number stage of transmitting control line driver unit is configured to receive the first clock pulse signal.

[0110] In the present embodiment, the first node N1, the second node N2, the third node N3, the fourth node N4 and the fifth node N5 are not real elements but virtual connecting nodes between components and elements. The first node N1 is a connecting node between the first PMOS transistor T1 and the second PMOS transistor T2. The second node N2 is a connecting node between the third PMOS transistor T3 and the fourth PMOS transistor T4. The third node N3 is a connecting node respectively connecting to the gate electrode of the fourth PMOS transistor T4, the gate electrode of the sixth PMOS transistor T6, the gate electrode of the seventh PMOS transistor T7 and the gate electrode of the ninth PMOS transistor T9. The fourth node N4 is a con-

necting node respectively connecting to the gate electrode of the fifth PMOS transistor T5, the gate electrode of the sixth PMOS transistor T6, the gate electrode of the seventh PMOS transistor T7, the gate electrode of the eighth PMOS transistor T8, the gate electrode of the eleventh PMOS transistor T11 and the second capacitor C2. The fifth node N5 is a connecting node respectively connecting to the gate electrode of the eighth PMOS transistor T8, the gate electrode of the ninth PMOS transistor T9, the gate electrode of the tenth PMOS transistor T10 and the first capacitor C1.

[0111] Hereinafter, particular circuit-conducted states and corresponding pulse waveform diagrams of the first stage of transmitting control line driver unit, at a first moment through a fifth moment, in the transmitting control line driver of the present disclosure are exhibited through FIGS. 5-10.

[0112] As illustrated in FIG. 5, at a first moment (corresponding to region “A” of FIG. 10) of the first stage of transmitting control line driver of the present disclosure, the first input terminal CKE1 is input with a low level, the second input terminal CKE2 is input with a high level, and the third input terminal “in” is input with a high level. Then, the first PMOS transistor T1 is cut-off; the second PMOS transistor T2 is conducted; the third PMOS transistor T3 is cut-off; the fourth PMOS transistor T4 is conducted; the fifth PMOS transistor T5 is cut-off; the sixth PMOS transistor T6 is conducted; the seventh PMOS transistor T7 is cut-off; the eighth PMOS transistor T8 is conducted; the ninth PMOS transistor T9 is cut-off; the tenth PMOS transistor T10 is cut-off; the eleventh PMOS transistor P11 is conducted; and finally, the signal output terminal “out” outputs a low level.

[0113] As illustrated in FIG. 6, at a second moment (corresponding to region “B” of FIG. 10) of the first stage of transmitting control line driver unit in the transmitting control line driver of the present disclosure, the first input terminal CKE1 is input with a high level, the second input terminal CKE2 is input with a low level, and the third input terminal “in” is input with a high level.

[0114] Then, the first PMOS transistor T1 is cut-off; the second PMOS transistor T2 is cut-off; the third PMOS transistor T3 is conducted; the fourth PMOS transistor T4 is conducted; the fifth PMOS transistor T5 is conducted; the sixth PMOS transistor T6 is cut-off; the seventh PMOS transistor T7 is conducted; the eighth PMOS transistor T8 is cut-off; the ninth PMOS transistor T9 is conducted; the tenth PMOS transistor T10 is conducted; the eleventh PMOS transistor P11 is cut-off; and finally, the signal output terminal out outputs a high level.

[0115] As illustrated in FIG. 7, at a third moment (corresponding to region “C” of FIG. 10) of the first stage of transmitting control line driver unit in the transmitting control line driver of the present disclosure, the first input terminal CKE1 is input with a low level, the second input terminal CKE2 is input with a high level, and the third input terminal “in” is input with a low level. Then, the first PMOS transistor T1 is conducted; the second PMOS transistor T2 is conducted; the third PMOS transistor T3 is cut-off; the fourth PMOS transistor T4 is conducted; the fifth PMOS transistor T5 is cut-off; the sixth PMOS transistor T6 is cut-off; the seventh PMOS transistor T7 is conducted; the eighth PMOS transistor T8 is cut-off; the ninth PMOS transistor T9 is conducted; the tenth PMOS transistor T10 is

conducted; the eleventh PMOS transistor P11 is cut-off; and finally, the signal output terminal “out” outputs a high level.

[0116] As illustrated in FIG. 8, at a fourth moment (corresponding to region “D” of FIG. 10) of the first stage of transmitting control line driver unit in the transmitting control line driver of the present disclosure, the first input terminal CKE1 is input with a high level, the second input terminal CKE2 is input with a low level, and the third input terminal “in” is input with a low level. Then, the first PMOS transistor T1 is conducted; the second PMOS transistor T2 is cut-off; the third PMOS transistor T3 is conducted; the fourth PMOS transistor T4 is cut-off; the fifth PMOS transistor T5 is conducted; the sixth PMOS transistor T6 is conducted; the seventh PMOS transistor T7 is cut-off; the eighth PMOS transistor T8 is conducted; the ninth PMOS transistor T9 is cut-off; the tenth PMOS transistor T10 is cut-off; the eleventh PMOS transistor P11 is conducted; and finally, the signal output terminal “out” outputs a low level.

[0117] As illustrated in FIG. 9, at a fifth moment (corresponding to region “E” of FIG. 10) of the first stage of transmitting control line driver unit in the transmitting control line driver of the present disclosure, the first input terminal CKE1 is input with a high level, the second input terminal CKE2 is input with a low level, and the third input terminal “in” is input with a low level. Then, the first PMOS transistor T1 is conducted; the second PMOS transistor T2 is conducted; the third PMOS transistor T3 is cut-off; the fourth PMOS transistor T4 is conducted; the fifth PMOS transistor T5 is cut-off; the sixth PMOS transistor T6 is conducted; the seventh PMOS transistor T7 is cut-off; the eighth PMOS transistor T8 is conducted; the ninth PMOS transistor T9 is cut-off; the tenth PMOS transistor T10 is cut-off; the eleventh PMOS transistor P11 is conducted; and finally, the signal output terminal “out” outputs a low level.

[0118] Furthermore, the states of the first input terminal CKE1, the second input terminal CKE2, the third input terminal “in” and the signal output terminal “out” correlated with the second stage of transmitting control line driver unit E2 through the fifth stage of transmitting control line driver unit E5 are illustrated in FIG. 10 (the pulse waveform of the first input terminal CKE1 of odd number stage of transmitting control line driver unit is identical with that of the first time sequence signal transmission line CK1, and the pulse waveform of the second input terminal CKE2 of odd number stage of transmitting control line driver unit is identical with that of the second time sequence signal transmission line CK2; while the pulse waveform of the first input terminal CKE1 of even number stage of transmitting control line driver unit is identical with that of the second time sequence signal transmission line CK1, and the pulse waveform of the second input terminal CKE2 of even number stage of transmitting control line driver unit is identical with that of the first time sequence signal transmission line CK1. Signals at each of input terminals and output terminals of the second stage of transmitting control line driver unit E2 through the fifth stage of transmitting control line driver unit E5 will not be described in details herein). The second stage of transmitting control line driver unit E2 through the fifth stage of transmitting control line driver unit E5 are delayed stage by stage, so as to drive the corresponding transmitting control lines, respectively.

[0119] The present disclosure further provides an OLED panel, which includes a signal controller, a data driver, a scan driver, a plurality of OLED pixels and a transmitting

control line driver as mentioned above. FIG. 11 illustrates a circuit block diagram of an OLED panel provided by the present disclosure. As illustrated in FIG. 11, as a basic structure, the light-emitting element display 1 includes an active matrix type light-emitting panel 2 and a signal controller 6 for controlling the entire light-emitting element display 1. The light-emitting element display 1 is a so-called active matrix driven type display device. The light-emitting panel 2 includes a transparent substrate made of, for example, borosilicate glass, quartz glass and other glasses which are high-temperature resistant during manufacturing process of transistors. A light-emitting unit 7 is formed on the transparent substrate. The light-emitting unit 7 is provided with a plurality of OLED pixels and is capable of emitting light so as to display images corresponding to image signals from the signal controller 6. The scan driver 3, the transmitting control line driver 4 and the data driver 5 are formed on the transparent substrate to drive the respective OLED pixels of the light-emitting unit 7. The scan driver 3, the transmitting control line driver 4 and the data driver 5 are connected so as to be capable of receiving data and control signal ϕ_s , ϕ_e and ϕ_d from the signal controller 6, respectively. Respective wirings and elements are formed on the transparent substrate to constitute the light-emitting panel 2.

[0120] In the light-emitting panel 2, m selective scan lines X_1, X_2, \dots, X_m are formed to be parallel to each other on the transparent substrate. In addition, m transmitting control lines E_1, E_2, \dots, E_m are formed on the transparent substrate so as to be arranged alternately with the selective scan lines X_1, X_2, \dots, X_m , respectively. These transmitting control lines E_1, E_2, \dots, E_m are parallel to and spaced from the selective scan lines X_1, X_2, \dots, X_m . In addition, data lines Y_1, Y_2, \dots, Y_n are formed on the transparent substrate to be substantially perpendicular to the selective scan lines X_1, X_2, \dots, X_m and the transmitting control lines E_1, E_2, \dots, E_m . The selective scan lines X_1, X_2, \dots, X_m , the transmitting control lines E_1, E_2, \dots, E_m and the data lines Y_1, Y_2, \dots, Y_n are made of at least one low impedance material selected from a group consisted of chromium, chromium alloy, aluminum, aluminum alloy, titanium and titanium alloy. The selective scan lines X_1, X_2, \dots, X_m and the transmitting control lines E_1, E_2, \dots, E_m may be formed from a same conductive film by using a patterning process. The data lines Y_1, Y_2, \dots, Y_n are intersected with the selective scan lines X_1, X_2, \dots, X_m and the transmitting control lines E_1, E_2, \dots, E_m . The selective scan lines X_1, X_2, \dots, X_m and the transmitting control lines E_1, E_2, \dots, E_m are insulated from the data lines Y_1, Y_2, \dots, Y_n by using, for example, a gate insulating film or a semi-conductive layer.

[0121] A plurality of organic EL elements E_{ij} are arranged on the transparent substrate in a form of matrix. One organic EL element is formed in each of regions enclosed by the data lines Y_1, Y_2, \dots, Y_n and the selective scan lines X_1, X_2, \dots, X_m . A driving circuit for supplying each of the organic EL elements with predetermined current is formed around each of the organic EL elements. One organic EL element and a driving circuit corresponding to this element constitute one OLED pixel P_{ij} of the light-emitting unit 2. In other words, one organic EL element is formed for each of the OLED pixels ($m \times n$ pixels).

[0122] As described in the foregoing, in the transmitting control line driver of the OLED panel, the signal output

terminal “out” of each stage of transmitting control line driver unit is coupled to one transmitting control line (E_1, E_2, \dots, E_m), and the signal output terminal “out” of each stage of transmitting control line driver unit provides a transmitting control signal to the transmitting control line (transmitting control transistor), which will not be repeated here.

[0123] The present disclosure further provides a display device, including a signal controller, a data driver, a scan driver, a plurality of OLED pixels and a transmitting control line driver as mentioned above. As described in the foregoing, in the transmitting control line driver of the display device, the signal output terminal “out” of each stage of transmitting control line driver unit is coupled to one transmitting control line (E_1, E_2, \dots, E_m), and the signal output terminal “out” of each stage of transmitting control line driver unit provides a transmitting control signal to the transmitting control line (transmitting control transistor), which will not be repeated here.

[0124] In summary, by using the transmitting control line driver in the present disclosure, the traditional four driving signals can be reduced to two driving signals, without increasing components or elements. In this way, the same function is achieved by less control signals; with the reduction of the control signal, the area of the circuit diagram can be saved, the area of the integrated circuit and also the number of the combined regions are decreased, the reliability is improved and wider operating spaces for components is allowed.

[0125] In the foregoing, particular embodiments of the present disclosure are described. It should be appreciated that the present disclosure is not limited to the above-mentioned specific embodiments. Various modifications and alternations can be made Within the scope defined by the claims by those skilled in the art, which would not depart from the substantive contents of the present disclosure.

1. A transmitting control line driver, including multiple stages of transmitting control line driver units, a single-pulse activating signal transmission line, a first time sequence signal transmission line and a second time sequence signal transmission line, wherein,

each stage of transmitting control line driver unit includes:

- a first transistor coupled between a first input terminal and a first node, the first transistor having a gate electrode coupled to a third input terminal;
- a second transistor coupled between the first node and a first power supply voltage, the second transistor having a gate electrode coupled to the first input terminal;
- a third transistor coupled between a second input terminal and a second node, the third transistor having a gate electrode coupled to the second input terminal;
- a fourth transistor coupled between the second node and a third node, the fourth transistor having a gate electrode coupled to the first node;
- a fifth transistor coupled between a fourth node and a signal input terminal, the fifth transistor having a gate electrode coupled to the second input terminal;
- a sixth transistor coupled between a second power supply voltage and the third node, the six transistor having a gate electrode coupled to the fourth node;
- a seventh transistor coupled between the second power supply voltage and the fourth node, the seventh transistor having a gate electrode coupled to the third node;

an eighth transistor coupled between the second power supply voltage and a fifth node, the eighth transistor having a gate electrode coupled to the fourth node;

a ninth transistor coupled between the fifth node and the first power supply voltage, the ninth transistor having a gate electrode coupled to the third node;

a tenth transistor coupled between the second power supply voltage and a signal output terminal, the tenth transistor having a gate electrode coupled to the fifth node;

an eleventh transistor coupled between the signal output terminal and the first power supply voltage, the eleventh transistor having a gate electrode coupled to the fourth node;

a first capacitor coupled between the second power supply voltage and the fifth node; and

a second capacitor coupled to the fourth node and the first input terminal,

wherein,

a signal output terminal of each stage of transmitting control line driver unit is coupled to a third input terminal of a next stage of transmitting control line driver unit;

a third input terminal of a first stage of transmitting control line driver unit is coupled to the single-pulse activating signal transmission line;

the first time sequence signal transmission line is coupled to first input terminals of odd number stages of transmitting control line driver units and is coupled to second input terminals of even number stages of transmitting control line driver units;

the second time sequence signal transmission line is coupled to second input terminals of odd number stages of transmitting control line driver units and is coupled to first input terminals of even number stages of transmitting control line driver units; and

the signal output terminal of each stage of transmitting control line driver unit is coupled to the third input terminal of the next stage of transmitting control line driver unit.

2. The transmitting control line driver of claim 1, wherein, the first transistor, the second transistor, the third transistor, the fourth transistor, the fifth transistor, the sixth transistor, the seventh transistor, the eighth transistor, the ninth transistor, the tenth transistor, and the eleventh transistor are all PMOS transistors.

3. The transmitting control line driver of claim 1, wherein, the first time sequence signal transmission line is configured to transmit a first clock pulse signal; the second time sequence signal transmission line is configured to transmit a second clock pulse signal; and the first clock pulse signal and the second clock pulse signal are not overlapped with each other.

4. The transmitting control line driver of claim 3, wherein, the second clock pulse signal is a half-period delay signal of the first clock pulse signal.

5. The transmitting control line driver of claim 1, wherein, the third input terminal of the first stage of transmitting control line driver unit is configured to receive a single-pulse activating signal.

6. The transmitting control line driver of claim 1, wherein, the signal output terminal of each stage of transmitting control line driver unit is further coupled to a transmitting control line.

7. An OLED panel, including a signal controller, a data driver, a scan driver, a plurality of OLED pixels and the transmitting control line driver according to claim 1.

8. A display device including a signal controller, a data driver, a scan driver, a plurality of OLED pixels and the transmitting control line driver according to claim 1.

9. The transmitting control line driver of claim 2, wherein, the first time sequence signal transmission line is configured to transmit a first clock pulse signal; the second time sequence signal transmission line is configured to transmit a second clock pulse signal; and the first clock pulse signal and the second clock pulse signal are not overlapped with each other.

10. The transmitting control line driver of claim 9, wherein, the second clock pulse signal is a half-period delay signal of the first clock pulse signal.

11. The transmitting control line driver of claim 2, wherein, the third input terminal of the first stage of transmitting control line driver unit is configured to receive a single-pulse activating signal.

12. The transmitting control line driver of claim 2, wherein, the signal output terminal of each stage of transmitting control line driver unit is further coupled to a transmitting control line.

13. An OLED panel, including a signal controller, a data driver, a scan driver, a plurality of OLED pixels and the transmitting control line driver according to claim 2.

14. An OLED panel, including a signal controller, a data driver, a scan driver, a plurality of OLED pixels and the transmitting control line driver according to claim 3.

15. An OLED panel, including a signal controller, a data driver, a scan driver, a plurality of OLED pixels and the transmitting control line driver according to claim 4.

16. An OLED panel, including a signal controller, a data driver, a scan driver, a plurality of OLED pixels and the transmitting control line driver according to claim 5.

17. An OLED panel, including a signal controller, a data driver, a scan driver, a plurality of OLED pixels and the transmitting control line driver according to claim 6.

18. A display device including a signal controller, a data driver, a scan driver, a plurality of OLED pixels and the transmitting control line driver according to claim 2.

19. A display device including a signal controller, a data driver, a scan driver, a plurality of OLED pixels and the transmitting control line driver according to claim 3.

20. A display device including a signal controller, a data driver, a scan driver, a plurality of OLED pixels and the transmitting control line driver according to claim 4.

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|----------------|--|---------|------------|
| 专利名称(译) | 发送控制线驱动器，具有该控制线驱动器的OLED面板和显示装置 | | |
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摘要(译)

发送控制线驱动器，具有该驱动器的OLED面板和显示装置。传输控制线驱动器包括多级传输控制线驱动器单元。第一时序信号传输线 (Ck 1) 在发送控制线驱动器单元和第二输入端的奇数级中耦合到第一输入端 (CKE 1) (CKE 2) 在传输控制线驱动器单元的偶数阶段。在发送控制线驱动器单元和第一输入端的奇数级中，第二时序信号传输线 (CK 2) 耦合到第二输入端 (CKE 2) (CKE 1) 在传输控制线驱动器单元的偶数级中。发送控制线驱动器单元的每级的信号输出端 (out) 耦合到发送控制线驱动器单元的后续级的第三输入端 (in)。

